MAHARAJA AGRASEN COLLEGE
University of Delhi
VASUNDHARA ENCLAVE, DElHI-ll0096

Curriculum Vitae of Faculty Members

First Name	Vandana	**Last Name**	Kumari
Designation	Assistant Professor	**Department**	Electronics
Date of Birth	6th June 1986	**Date of Joining**	August 2014
Residential Address	R Z-35-36, Vishu Vihar, Uttam Nagar, New Delhi-59		
Contact No	9971657377	Email Id	

Education

	Institution	**Year**	**Details**
Ph.D	University of Delhi	2014	Micro-Electronics
Masters	University of Delhi	2009	Electronics
Graduation	University of Delhi	2006	B. Sc (Gen) Electronics

Career Profile

Organization/ Institution	**Post Held**	**Adhoc/Temp/ Permanent**	**From**	**To**	**Total Experience**
Maharaja Agrasen College, University of Delhi	Assistant Professor	Adhoc	August 2014	Till Date	5 Years 11 Months

Administrative Assignments if any
Member of Student Aid, Annual Activity and Alumni Committee

Teaching Experience (Subjects/Courses Taught)
B. Sc. (H) Electronics: Semiconductor Devices, Network Analysis, Communication Electronics, Control system, Machines

Areas of Interest/Specialization: Modeling and Simulation of Nanoscale Devices, Semiconductor Devices
Digital and Analog Electronics & Communication

Details of Published Research Papers, Books, Monographs, Reviews, Chapter in Books, Translations and Creative Positons held

Year of Publications	Title	ISBN No	Publisher	Co-Authors

h-Factor-7

1. "Temperature Dependent Drain Current Model for Gate Stack Insulated Shallow Extension Silicon On Nothing (ISESON) MOSFET For Wide Operating Temperature Range," **Vandana Kumari**, Manoj Saxena, Mridula Gupta and R. S. Gupta, ***Microelectronics Reliability (MER)***, Vol. 52, pp. 974-983, 2012. *Impact Factor (**1.137**)* ISSN: **0026-2714 Citation 14**
2. "Simulation Study of Insulated Shallow Extension Silicon On Nothing (ISESON) MOSFET for High Temperature applications," **Vandana Kumari**, Manoj Saxena, R. S. Gupta and Mridula Gupta, ***Microelectronics Reliability (MER)***, Vol. 52, pp. 1610-1612, 2012. *Impact Factor (**1.137**)* ISSN: **0026-2714 Citation 10**
3. "Two Dimensional analytical Drain Current Model for Double Gate MOSFET Incorporating Dielectric Pocket (DP-DG)," **Vandana Kumari**, Manoj Saxena, R.S. Gupta, and Mridula Gupta, ***IEEE***

Transactions On Electron Device (TED), Vol. 59, no. 10, pp. 2567 - 2574, 2012. *Impact Factor (**2.062***), ISSN: **0018-9383. Citation 24**

4. "Digital Circuit Analysis of Insulated Shallow Extension Silicon On Void (ISESOV) FET for Low Voltage Applications" **Vandana Kumari**, Manoj Saxena, R. S. Gupta and Mridula Gupta, ***SPIE Digital Library***, Vol. 8549, pp. 854905-1-6, 2012. *Impact Factor **(0.88),*** DOI: 10.1117/12.925533
5. "Analog and digital Performance Assessment of Empty Space in Double Gate (ESDG) MOSFET: A Novel Device Architecture" **Vandana Kumari**, Manoj Saxena, R.S. Gupta, and Mridula Gupta, ***Journal of Computational and Theoretical Nanoscience (JCTN),*** Vol. 10, no. 2, pp.389-398, 2013. *Impact Factor **(0.912),*** ISSN: **1546-1955** (Print): EISSN: **1546-1963** (Online) **Citation 3**
6. "Investigation of Empty Space in Nanoscale Double Gate (ESDG) MOSFET for High Speed Digital Circuit Applications**" Vandana Kumari**, Manoj Saxena, R.S. Gupta, and Mridula Gupta, ***Journal of Semiconductor Technology and Science (JSTS),*** Vol. 13, no. 2, pp.127-138, 2013. *Impact Factor (0.366),* ISSN: **1598-1657**. **Citation 1**
7. "Circuit Level Implementation for Insulated Shallow Extension silicon On Nothing (ISE-SON) MOSFET: A Novel Device architecture" **Vandana Kumari**, Manoj Saxena, R.S. Gupta, and Mridula Gupta, ***IETE Journal of Research (JR), Vol. 59, no.4, pp 404-409, 2013***. *Impact Factor **(0.2),*** ISSN **0377-2063** (Print), **0974-780X** (Online)
8. "Performance Investigation of Insulated Shallow Extension Silicon On Nothing (ISE-SON) MOSFET for Low Voltage Digital Applications," **Vandana Kumari**, Manoj Saxena, R.S. Gupta, and Mridula Gupta, ***Journal of Semiconductor Technology and Science, Vol. 13, no.6, pp. 622-634, 2013.*** *Impact Factor (0.366)*. ISSN: **1598-1657**. **Citation 2**
9. "Comparative Study of Silicon On Nothing and III-V On Nothing Architecture for High Speed and Low Power Analog and RF/Digital Applications," **Vandana Kumari**, Manoj Saxena, R.S. Gupta, and Mridula Gupta, ***IEEE Trans. On Nanotechnology, Vol. 12, no.6, pp. 978-984, 2013.*** *Impact Factor **(1.80)**. ISSN:* **1536-125X**. **Citation 5**
10. "Analytical Modeling of Dielectric Pocket Double Gate (DP-DG) MOSFET Incorporating Hot Carrier Induced Interface Charges" **Vandana Kumari**, Manoj Saxena, R.S. Gupta, and Mridula Gupta, ***IEEE Transactions on Device and Material Reliability,*** *Vol. 14, no.1, pp. 390-399, 2014. Impact Factor **(1.516)**.* ISSN: **1530-4388. Citation 13**
11. "Investigation of Electrostatic Integrity of Nanoscale Dual Material Gate Dielectric Pocket Silicon On Void (DMGDPSOV) MOSFET for Improved Device Scalability**" Vandana Kumari**, Manoj Saxena, R.S. Gupta, and Mridula Gupta, **IEEE Trans. On Nanotechnology,** ***Vol. 13, no.4, pp. 667-675, 2014.*** *Impact Factor **(1.80).** ISSN:* **1536-125X**. Citation: 4
12. "Modeling and Simulation of Double Gate Junctionless Transistor Considering Fringing Field Effects**" Vandana Kumari**, Neel Modi, Manoj Saxena, and Mridula Gupta, **Solid State Electronics,** ***Vol. 107, pp.20-29, 2015.*** *Impact Factor **(1.514),*** ISSN: **0038-1101** ***Citation: 22***
13. **"**Theoretical Investigation of Dual Material Junctionless Double Gate Transistor for Analog and Digital Performance**" Vandana Kumari**, Neel Modi, Manoj Saxena, and Mridula Gupta, **IEEE Trans. On Electron Devices,** ***Vol. 67, no.7 pp.2098-2105, 2015.*** *Impact Factor (**2.062***), ISSN: **0018-9383.** ***Citation: 20***
14. "Nanoscale-RingFET: An Analytical Drain Current Model Including SCEs" Sachin**, Vandana Kumari**, Sanjeev Singh, Manoj Saxena, and Mridula Gupta, **IEEE Trans. On Electron Devices,** ***Vol. 62, no.12 pp.3965-3972, 2015.*** *Impact Factor (**2.062***), ISSN: **0018-9383.** ***Citation: 6***
15. "**Modeling and Simulation of Nanoscale Lateral Gaussian Doped Channel Asymmetric Double Gate MOSFET**" ***Vandana Kumari,*** *Manoj Saxena and Mridula Gupta,* **Journal of NanoResearch** ***Vol. 36, pp.51-63, 2016***. *Impact Factor (**0.52***) , **ISSN: 1661-9897.** ***Citation: 2***
16. **"Nanoscale T-shaped Double Gate DG MOSFET: Numerical Investigation for Analog/RF and Digital Performance"** ***Vandana Kumari,*** *Aravindin Ilango, Manoj Saxena and Mridula Gupta, Superlattices and Microstructures,* ***Vol. 89, pp.97-111, 2016***. *Impact Factor (**2.097***), **ISSN: 0749-6036**
17. **"Underlapped FinFET on insulator: Quasi3D analytical model" Vandana Kumari,** K. Shermetha, Manoj Saxena and Mridula Gupta, Solid State Electronics, Vol 129, pp. 138-149, 2017. ISSN: 0038-1101 ***Citation: 5***
18. **Sub-threshold Drain Current model of Double Gate RingFET (DG-RingFET) Architecture: An Analog and Linearity Performance Investigation for RFIC Design"** Sachin**, Vandana Kumari,** Sanjeev Singh, Manoj Saxena and Mridula Gupta, *IETE Technical Review* (TR), pp. 169-179, 2017. https://dx.doi.org/10.1080/02564602.2016.127017, ***Citation: 3***
19. **"Analytical Drain Current Model for Gate and Channel Engineered RingFET (GCE-RingFET)"** Sachin**, Vandana Kumari,** Sanjeev Singh, Manoj Saxena and Mridula Gupta, Superlattices and Microstructure, Vol. 111, pp. 1113-1120, 2017. Citation: 1
20. "**Variability Investigation of Double Gate JunctionLess (DG-JL) Transistor for Circuit Design Perspective**," Vandana Kumari, Manoj Saxena and Mridula Gupta, VLSI Design and Test symposium (VDAT-2017), Communications in Computer and Information Science, vol 711, pp 496-503. Springer, Singapore 2017. ISBN: 978-981-10-7470-7. ***Citation: 1***
21. **Empirical Model for Nonuniformly Doped Symmetric Double-Gate Junctionless Transistor"** Vandana Kumari, Ayush Kumar, Mridula Gupta and Manoj Saxena, **IEEE Trans. On Electron Devices**, Vol. 65, pp. 314-321, 2018. ***Citation: 13***
22. **"Reconnoiter the leavening of Skin Deep Insulated Extension on Analog Performance of RingFET (SDIE-RingFET)"** Sachin**, Vandana Kumari,** Sanjeev Singh, Manoj Saxena and Mridula Gupta, **AEU-**

Internation Journal of Electronics and Communication, Vol 83, pp. 67-72, 2018. 1434-8411 Citation: 1

23. "**Study of Gaussian Doped Double Gate JunctionLess (GD-DG-JL) Transistor Including Source Drain Depletion Length: Model for Sub-threshold Behaviour**" Vandana Kumari, Ayush Kumar, Mridula Gupta and Manoj Saxena, **Superlattices and Microstructure**, Vol. 113, pp. 57-70, 2018. Citation: 6
24. "**Study of Extended Back Gate Double Gate JunctionLess Transistor: Theoretical and Numerical Investigation**" Vandana Kumari, Abhineet Sharan, Mridula Gupta and Manoj Saxena, Springer Proceedings in Physics, vol 215, pp 633-642, Springer, Cham, 2019. ISBN 978-3-319-97604-4
25. "**Optically Controlled Silicon On Nothing MOSFET-Numerical Simulation**" Vandana Kumari, Mridula Gupta and Manoj Saxena, Springer Proceedings in Physics, vol 215, pp. 1071-1076. Springer, Cham, 2019. ISBN 978-3-319-97604-4
26. "**Threshold Voltage Investigation of Recessed Dual-Gate MISHEMT: Simulation Study**", Preeti Singh, Vandana Kumari, Manoj Saxena and Mridula Gupta, Communications in Computer and Information Science, vol 892. pp 380-393, Springer, Singapore, 2019. ISBN978-981-13-5950-7
27. **"Temperature Based Analysis of 3-Step Field Plate AlGaN/GaN HEMT using Numerical Simulation"** Neha, Vandana Kumari, Manoj Saxena and Mridula Gupta, **Advances in Natural Sciences: Nanoscience and Nanotechnology , Vol. 10, no.4, 2019.** Citation: 0
28. **TCAD-Based Assessment of Dual-Gate MISHEMT with Sapphire, SiC, and Silicon Substrate,** Preeti Singh, Vandana Kumari, Manoj Saxena and Mridula Gupta, IETE Technical Review, online available on 22 Dec. 2019. Citation:0
29. **Sensitivity Assessment of RingFET Architecture for the Detection of Gas Molecules: Numerical Investigation,** Vandana Kumari, Manoj Saxena and Mridula Gupta, IETE Technical Review, online available on 10 March. 2020, Citation:0
30. **Assessment of Dual-Gate AlGaN/GaN MISHEMT for high temperature DC to DC converter"** Preeti Singh, Vandana Kumari, Manoj Saxena and Mridula Gupta, Superlattices ad Microstructures, Vol. 144, pp. 106574, 2020.

Participation in conferences, seminars, workshops, refreshers, orientation courses attended, summer institutes etc.

State/National International	Title	Organization	Period

1. 18th **Workshop and IEEE EDS Mini-Colloquium on Nanometer CMOS Technology**, 4th – 5th June 2009, at University of Delhi south Campus, India.
2. **Two Days National Workshop On Fiber Optics and Applications**, 28th – 29th Nov. 2009, at University of Delhi south Campus, India.
3. 12th **International symposium On Microwave and Optical Technology** (ISMOT-2009), 16th – 19th Dec. 2009 at Hotel Ashok, New Delhi, India.
4. **First National Workshop On Recent Trends in Semiconductor Devices and Technology**, 12th - 13th February, at Deen Dayal Upadhyaya College, University of Delhi, New Delhi, India.
5. 4th Indian Nanoelectronics User's Programme INUP Familiarization Workshop **International Winter School on Nano-scale Materials and Devices** (IWNMD 2010), 13th – 17th Dec. 2010, at IIT Bombay, India.
6. National Conference and Workshop On **Recent Advances in Modern Communication Systems and Nanotechnology (**NCMCN- 2011**),** 6th -8th Jan. 2011, at Jaipur, India.
7. **International IEEE Student's Technology Symposium**, 14th -16th January 2011, IIT Kharagpur, India.
8. **VLSI Design and Test symposium (**VDAT-2011**),** 7th – 9th July 2011, at Pune, India.
9. **National Seminar on Recent Advances in Microelectronics Devices**, 19th – 20th August 2011, at Maharaja Agrasen Institute of Technology, Delhi, India.
10. **International Workshops on Physics of Semiconductor Devices** (IWPSD-2011), 19th – 22nd December 2011, IIT Kanpur, India.
11. **International Conference on Nano Science and Technology (**ICONSAT-2012**),** January 20th -23rd, 2012 at Hyderabad, India.
12. Mini-Colloquia on "**Compact Modelling Techniques for Nanoscale Devices and Circuit Analysis**" *Organized by IEEE EDS-Delhi Chapter, New Delhi,* Sponsored by the IEEE Electron Devices Society under its Distinguished Lecturer Program, 14th -15th March, 2012 at University of Delhi South Campus, New Delhi, India.
13. **International Conference on Circuit Devices and Systems (**ICDCS-2012**),** 15th -16th March, 2012 at Coimbatore, India.
14. **International Workshop On Device Modeling for Microsystems MOS-AK/GSA INDIA**, 17th – 18th March 2012, at Jaypee University, Noida, India.
15. **Seminar On Recent Advances in Microwave and Photonic Devices** on 4th October 2012, at Maharaja Agrasen Institute of Technology, Delhi, India.
16. **International Conference on Nanotechnology Innovative Materials, Processes, Product and Applications** (NANOCON 2012), 18th -19th Oct, 2012, at Pune, Maharashtra, India.

17. **International Conference on Emerging Electronics** (ICEE 2012), 15th -17th December, 2012, at IIT Bombay, India.
18. **National Conference on Recent Developments in Electronics** (NCRDE-2013), 18th -20th January, 2013, at University of Delhi South Campus, New Delhi, India.
19. One day Short Course on **"Nanotechnology Journey from Quantum Physics to Nanoengineering"** SP Jain Centre, University of Delhi South Campus, New Delhi, India, January 28, 2014, by prof. Vijay Arora, Wilkes University, U.S.A.
20. Fourth National workshop on "**Recent Trends in Semiconductor Devices and Technology**" at Deen Dayal Upadhyaya College, University of Delhi, New Delhi, September 12-13, 2014.
21. National Conference on **"Striving & Thriving Towards Diffusion of Student-driven Research in Science and Technology for Inspired Learning"** at Maharaja Agrasen College, University of Delhi, New Delhi, India, October 16-17, 2014.
22. **International conference of recent advances in Nanoscience and Nanotechnology** (ICRANN, New Delhi, India) December 15-16, 2014.
23. CSIR sponsored Second Lecture Workshop on "**Trans-disciplinary Areas of Research and Teaching**" by Shanti Swaroop Bhatnagar Awardee, at Deen Dayal Upadhyaya College, University of Delhi, New Delhi, January 30-31, 2015.
24. **International Workshops on Physics of Semiconductor Devices** (IWPSD-2015), 7th – 10th December 2015, IISc Bangalore, India.
25. **International Conference on Emerging Electronics** (ICEE 2016), 27th -30th December, 2016, at IIT Bombay, India.
26. **VLSI Design and Test symposium (**VDAT-2017**),** 30th June– 2nd July 2017, at IIT Roorkee, Roorkee, India.
27. International Workshop on Physics of Semiconductor Devices IWPSD, New Delhi, Poster Presentation, 11-15 Dec 2017.
28. *IEEE Electron Device Kolkata Conference (2018 EDKCON),* Kolkata, India 24th-25th November,2018.
29. IMRAC-2019, 13th – 15th Dec. 2019, IIT Bombay, India

Professional Societies Memberships:

- **Joint Secretary**- IEEE EDS Delhi Chapter 2019-till date
- **Treasurer**- IEEE EDS Delhi Chapter 2015-2018
- Member of Institute of Electrical and Electronic Engineering ***IEEE***
- **Member** of ***IEEE*** Electron Device Society ***IEEE-EDS***
- **Reviewer** of ***IOP Nanotechnology*** Journal
- **Reviewer** of ***Journal of Electrical Engineering and Electronic Technology***

I certify that the information given above is correct and factual to the best of my knowledge.

Signature: Dr. Vandana Kumari